REMARKS

Applicants appreciate the notification of allowable subject matter, i.e., that claims 2, 10, and 17 are merely objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Claims 1-20 are pending in the application. Claims 1 and 9 have been amended by the present amendment. The amendments are fully supported by the application as originally filed (see, e.g., specification at page 7, last three paragraphs to page 8, first paragraph; FIGS. 6A-6B).

As amended, claims 1 and 9 recite a lead frame and a semiconductor package including: a die pad, and a plurality of grounding portions formed on at least a side of the die pad, each of the grounding portions having a grounding surface and a ground pad formed on the grounding surface, such that a plurality of grounding wires are respectively bonded to the ground pads of the grounding portions and a semiconductor chip for transmitting ground signals.

For example, as shown in FIGS. 6A and 6B, a plurality of grounding portions 51 protrude from a die pad 50, each grounding portion having a grounding surface 51a (see specification at page 7, last paragraph). Because of a height difference between the top surface of the die pad 50 and a ground pad 51c formed on the grounding surface 51a, when the die pad 50 is subject to high-temperature processes, the grounding portion 51 would be less likely to deform, as compared to conventional arrangements (see page 8, first paragraph).

Claims 1, 3, 9, 11, and 16 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 6,208,023 to Nakayama et al. ("Nakayama"), or under 35 USC 102(e) as being anticipated by U.S. Patent 6,853,059 to Jang. The remaining claims also were rejected over prior art. These rejections are respectfully traversed.

The Nakayama and Jang references do not teach or suggest a lead frame or semiconductor package in which a plurality of grounding portions are formed on at least a side of a die pad, as recited in claims 1 and 9. FIG. 6B of the application provides an example of a **plurality** of grounding portions 51 formed along a side of a die pad 50.

Referring to FIGS. 1(a)-1(b) of Nakayama, a single thickness-reduced side portion 12a is provided on a longer side of the die pad 12 (see column 10, lines 43-46). The thickness-reduced side portion 12a extends along the entire length of the longer side of the die pad 12 (FIG. 1(a)). Therefore, Nakayama does not teach or suggest a **plurality** of grounding portions formed on at least a side of a die pad, as recited in claims 1 and 9.

Moreover, the thickness-reduced side portion 12a in Nakayama is similar to PRIOR ART FIGS. 5A-5B of the application (see page 3, last paragraph to page 4, first paragraph). By providing a single thickness-reduced portion or a step-like part according to conventional technology, deformation of the die pad and breaking of grounding wires due to uneven thermal expansion under high-temperature conditions becomes more prevalent.

Referring to FIGS. 1-2 of Jang, a continuous ground ring 262 is formed in a half-etched section 150 of a chip paddle 80, and is positioned between a semiconductor chip 20 and a plurality of leads 230 (see column 3, lines 58-61).

However, Jang does not teach or suggest a **plurality** of grounding portions formed on at least a side of a die pad, as recited in claims 1 and 9. Moreover, the continuous ground ring 262 in Jang is similar to the prior art illustrated in FIGS. 2A-2B, 3A-3B, and 4A-4B of the application (see page 2, third paragraph to page 3, third paragraph). The continuous ground ring of Jang and the prior art is subject to deformation during a high-temperature fabrication process, and possible short-circuiting of electrical connections between the chip and leads.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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